Cont A7

24. The apparatus of claim 14 wherein said parasitic capacitance appears between said input and ground.

25. The apparatus of claim 6 wherein the capacitance of the detection circuit has one terminal directly connected to one terminal of the parasitic capacitance.--

REMARKS

The present application contains claims 1 through 25. Claim 5 has been amended and claims 18-25 have been newly added.

The rejection of claims 5 through 7 as failing to comply with 35 U.S.C. § 112 is hereby respectfully traversed.

Claim 5 has been amended to delete the recitation "that would be" to provide a positive recitation.

It is submitted that claim 5 is now in compliance with 112 and that claims 6 and 7 are also in compliance because they now depend from claim 5 as amended.

In view of the foregoing comments it is submitted that rejection of claim 5 through 7 under 112 should be withdrawn.

Claims 1 through 13 have been rejected under 35 U.S.C. § 102(b) as anticipated by Cave et al. (Patent '389). This rejection is respectfully traversed.

The Examiner states that, regarding claims 1 and 12, Fig. 3 of Cave shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of: detecting a direction of change in voltage of input signal Vin (34); and introducing a current (I) to the parasitic capacitance (C1) to compensate for current of the input signal charging the parasitic capacitance responsive to detection of a positive edge of said input signal; when the input signal Vin goes high, transistor (34) is turned on and transistor (42, having the collector connected to node 40) charges the parasitic capacitance (C1) with current I.

It should be noted that the displacement current provided in the circuit of Cave et al. utilizes a second parasitic capacitance C2. The current in the circuit branch comprised of the parasitic capacitance C2 is equal to C2 dv/dt as recited at lines 10 through 15, column 4 of Cave et al. Transistor 42, which is unfortunately not numbered in Fig. 3 but is clearly described at lines 5 through 19, column 4 of Cave et al., develops a collector current which is C2 β dv/dt which is described as being "β times" more current inserted into node 40 than is pulled out of node 40 by the parasitic capacitance C1 then the voltage drops. Thus, Cave

et al. **requires** that a **larger** current flow into node 40 than flows out of node 40 to prevent oscillation.

Cave is exclusively concerned with the situation that, because parasitic capacitance C1 is coupled between node 40 and the output V_{OUT}, when the voltage drops at V_{OUT}, C1 causes the voltage at 40 to drop which will cause transistor 22 to turn on again, leading to unwanted oscillation.

In the present invention, the objective is to prevent distortion of the input signal at the output. Such distortion **will** occur in Cave et al. since there is **inequality** between current C1 dv/dt and the current C2 β dv/dt. Claim 1 recites that distortion is reduced by introducing a current to the parasitic capacitance to compensate for the current of the input signal charging the parasitic capacitance. It can clearly be seen that Cave et al. overcompensates. It is thus submitted that claim 1 patentably distinguishes thereover.

Regarding claim 2, in view of the fact that claim 2 depends from claim 1 and carries all of its limitations, it is submitted that claim 2 patentably distinguishes over Cave et al. for the same reason set forth hereinabove with regard to claim 1.

Regarding claims 3 and 13, it is submitted that MOSFET transistor 34 is not a detection circuit for preventing discharge of the parasitic capacitance. Transistor 34 is

simply a means of introducing the input signal into the circuit. It is the interaction of C2 with the transistor 42 that provides the overcompensation.

Regarding claims 4 and 11, as was pointed out hereinabove with respect to claims 3 and 13, it is submitted that transistor 34 is not a detecting circuit. More specifically, it should be noted that Cave et al. uses a parasitic capacitance C2 to detect the change in voltage at the output point. Nevertheless, Cave et al. employs a technique which develops a signal which is

β x larger than the current in the parasitic capacitance C1.

The Examiner's statement that a transistor 34 detects a change in the voltage of the input signal and changes an impedance of a parallel termination circuit is not understood, especially since there is no element "2" referred to by the Examiner. Assuming that the Examiner intended to mean the elements 32, 38 and 22, there is no teaching in Cave et al. that the impedance of these circuit elements change, especially in light of the fact that there is no description whatsoever of the "control circuit" 38. In addition, there is no description nor is there any objective recited in Cave et al. that the change in the parallel termination circuit 2, 38 and 22 reduces distortion of the input signal. Also 2, 3, 8 and 27 are <u>not</u> a termination circuit which terminates a transmission line as is the case in the present invention. It should be noted that the objection of Cave et al. is to prevent oscillation at the

output. The objective of Cave et al. is to introduce a current which is β times greater than the current through the parasitic capacitor C1 to prevent oscillation when the "vertical transistor" 22 is turned off. There is no teaching of nor is there any objective of preventing distortion of an input signal.

Regarding claim 5, it is again submitted that the circuit 34 is **not** a detection circuit.

Regarding claim 6, it is submitted that since transistor 34 is not part of the detection circuit, the capacitance C2 is not part of transistor 34.

Regarding claim 7, even assuming that circuit 30 is an input/output device, it is submitted that claim 7, which carries all the limitations of claim 5, patentably distinguishes over Cave et al. for the same reasons set forth hereinabove with regard to claim 5.

Regarding claim 8, it should be noted that when a negative going signal applied to the input of transistor 34 causes transistor 34 to turn off, current flows into node 40 through transistor 42 thus adding to the input signal, whereas claim 8 recites that the detection circuit prevents current from the parasitic capacitance to be added to the input signal. Thus, the present invention is the direct opposite of Cave et al.

It is submitted that claims 9 and 10 patentably distinguish over Cave et al. since these claims depend from claim 8 and carry all its limitations and hence that these claims

patentably distinguish over Cave et al. for the same reasons set forth herein above in regard to claim 8.

In addition to the above, it should be noted that Cave et al. is specifically limited to teaching a circuit in which the P+ substrate 12 which is utilized as V_{OUT}, the parasitic capacitance is coupled between the V_{OUT} terminal and the base electrode transistor 32.

In contrast, the parasitic capacitance of the present invention has one terminal directly coupled to ground and the other terminal coupled to the input terminal and hence is **not** coupled directly to the output terminal. Note figures 2A-2D and 3 of the present application. These limitations are found in new claims 18 and 19 which respectively depend from claims 1 and 3; claims 4 and 5; claims 20 through 22 which respectively depend from claims 8, 11 and 12; and claims 23 and 24 which respectively depend from claims 13 and 14. These features are not taught or even remotely suggested in Cave et al. and it is submitted that amended claims 4 and 5 and new claims 18 through 24 all patentably distinguish over Cave et al.

It should further be noted that whereas the parasitic capacitance C1 is coupled to the input node 40, the detector capacitance C2 is not directly connected to the input. This feature is set forth in new claim 25 and it is submitted that claim 25, which depends from claim 6

and carries all its limitations, further patentably distinguishes over Cave et al. for these added reasons.

Claims 14 through 17 have been rejected under 35 U.S.C. § 102(b) is anticipated by Ooishi (Patent '656). This rejection is respectively traversed.

The Examiner states that Figure 22 of Ooishi shows an apparatus for reducing distortion of a signal applied to an input (OUT) of a circuit operating at high frequency and having a parasitic capacitance, comprising: a first circuit element 162 for selectively providing current to the parasitic capacitance Cm, which is included in line 110 and 150 when QP (PQ?) and 162 are turned on; a second circuit element 163 for selectively preventing discharge of the parasitic capacitance Cm into the input, i.e. OUT, when NQ and 163 are turned off, and a control circuit G monitoring the input signal for respectively turning on the first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of the input signal is detected.

Firstly, there is no teaching in Ooishi that there is a parasitic capacitance in the input circuit nor is there any teaching of the location of a parasitic capacitance and there is further no teaching in Ooishi of either circuitry or a device for suppling current to the parasitic

capacitance when in the first operating state and for preventing current from flowing from the parasitic capacitance when in a second operating state.

Ooishi requires main source and sub-source lines 100 and 110 and main ground and sub-ground lines 140 and 150 and requires inputs equal to VCH and VSL to be sure that one of the current regulating elements 162 and 163 are alternately turned off. In addition, there is no teaching of compensating for the harmful effect of a parasitic capacitance between the input IN in Fig. 22 and the line VC (or VCH) in Fig. 22.

In addition to the above, it is submitted that neither circuit element 162 nor circuit element 163 provide any current to gate circuit G nor to any parasitic capacitance since there is no parasitic capacitance described in the Ooishi patent. It should be noted that the terminal of gate circuit G between the transistors PQ and NQ is an **output** coupled to the control gates (i.e. **inputs**)of the transistors 167 and 168 which is the direct opposite of the description set forth by the Examiner. Control circuit 162 serves to either reduce the voltage between the main source line 100 and the sub-source line 110 or, when turned off in another state serves to enable the clamping circuit 160 to clamp a specific voltage difference across the main source line 100 and sub-source line 110. Note that the input to the control gate of transistor 165 is a fixed value. Transistor 168 operates in a similar fashion to either alter the voltage between the sub-ground line 150 and the main ground line 140 or alternatively when turned off allows the transistor 166 to control the voltage difference between the main and the sub-

ground lines 140 and 150. It should be noted that a fixed voltage level is applied to the control electrode of transistor 166. It is clear that neither the transistor 167 nor the transistor 168 has any terminal coupled to the input IN and this is likewise true of the transistors 165 and 166. It is submitted that this reference neither teaches nor remotely suggests any of the novel features of claim 14.

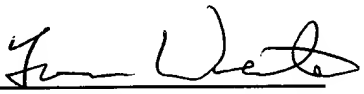
Claims 15 through 17 depend from claim 14 and carry all of its limitations and therefore patentably distinguish over Ooishi for the same reasons set forth hereinabove with regard to claim 14.

In view of the foregoing, it is submitted that claims 1 through 17 patentably distinguish over the art of record and reconsideration and allowance of these claims are earnestly solicited and that newly added claims 18 through 25 patentably distinguish over the cited prior art and consideration and allowance of these claims are earnestly solicited.

Favorable action is awaited.

Respectfully submitted,

Drapkin et al.

By 

Louis Weinstein, Esquire
Registration No. 20,477
(215) 568-6400

Volpe and Koenig, P.C.
Suite 400, One Penn Center
1617 John F. Kennedy Boulevard
Philadelphia, PA 19103

LW/gms
Enclosure

Application No.: 09/651,944
Examiner: Hiep Nguyen

37 CFR §1.121(b)(1)(iii) and (c)(1)(ii) SPECIFICATION AND CLAIM AMENDMENTS- MARKED UP VERSION

IN THE SPECIFICATION

Page 2, please delete the paragraph between lines 5 through 7 and insert therefor:

--It is therefore, one object of the present invention, [is] to provide an apparatus for compensating for impedance mismatch between interconnected circuits operating at high frequencies.--

Page 2, please delete the paragraph at line 27 and insert therefor:

--Figure 4 shows a timing diagram useful to understand the Figure 3 schematic.--

Page 3, please delete the paragraph between lines 2 through 9 and insert therefor:

--Transmitter output impedance and transmission line impedance matching and termination technique is a concern if the signals rising/falling timing is comparable with the flight time through the transmission line. In some electronic interfaces, it is very important that the impedance of a transmitter match the characteristic line impedance and that a receiver connected thereto be capable of operating like an open circuit. Still other interfaces employ additional line termination techniques in order to prevent [from] reflection at the receiving end. In the later case, the additional terminated device or devices can be installed at the receiving end to minimize possible sources of reflection.--

Page 5, please delete the paragraph between lines 18 through 20 and insert therefor:

--Figure 2B shows a slightly more detailed schematic as compared with Figure 2A, in which the tracking system 10 is a dv/dt analyzer operating a charge pump 11 to compensate for charging or discharging of parasitic capacitor C_P.--

Page 5, please delete the paragraph between lines 21 through 27 and insert therefor:

--With reference to Figure 2C, the input signal is shown applied to the I/O pad P through the transmission line represented by the impedance Z_L. The tracking system employs a capacitor C_T having one terminal coupled to one terminal of the parasitic capacitance C_P and the other terminal coupled between a current source 12 and an NMOS transistor 14 having its gate coupled to its drain, as well as with the gate of the second NMOS transistor 16. A PMOS transistor 18 has its drain and gate coupled to a drain of NMOS transistor 16 as well as with the gate of the second PMOS transistor 20.

IN THE CLAIMS

Please amend claim 5 as follows:

5. (Amended) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for current from said input signal [that would be] diverted to said parasitic capacitance due to a positive edge of said input signal.

Please add the following new claims 18-25:

--18. The method of claim 1 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

19. The method of claim 3 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

20. The apparatus of claim 9 wherein said parasitic capacitance appears between said input and ground.

21. The apparatus of claim 11 wherein said parasitic capacitance appears between said input and ground.

22. The apparatus of claim 12 wherein said parasitic capacitance appears between said input and ground.

23. The method of claim 13 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

24. The apparatus of claim 14 wherein said parasitic capacitance appears between said input and ground.

25. The apparatus of claim 6 wherein the capacitance of the detection circuit has one terminal directly connected to one terminal of the parasitic capacitance.--